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Compact Modelling of Wafer Level Chip-Scale Package via Parametric Model Order Reduction.

INTRODUCTION AND MOTIVATION

The interconnect reliability of a packaged chip on the printed circuit board is a major requirement that should be met for assembling microelectronics. EU project COMPAS concentrates on thermomechanical reliability issues in high-tech systems, such as motor control units for automated factories, smart infrastructures or autonomous vehicles. COMPAS aims to develop novel, compact models and ultra-compact digital twins by using advanced mathematical methods of model order reduction. In this paper we present a successful application of parametric model order reduction for constructing a compact model of a packaged chip starting from the full order finite element model (see Fig.1). Temperature dependent Young modulus of an isotropic material, is preserved in the symbolic form within the compact model.

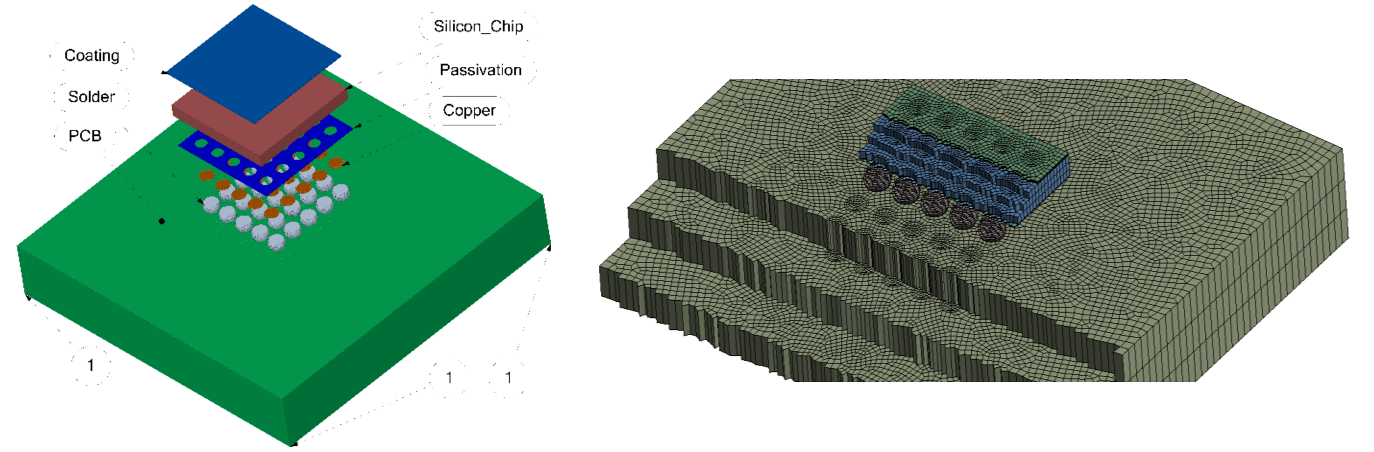

Fig. 1. A waver level chip-scale package setup and finite element mesh.

PARAMETRIZED FINITE ELEMENT MODEL AND IT'S REDUCTION VIA PROJECTION

Identification of the system matrices that result from the finite element analysis is a crucial pre-step for the model reduction process.

- Young's modulus E within the system matrices and the load vector:

$$([K_e]+[K_e^f])\{U\}-\{F_e^{th}\}=\mathbf{0},[K_e]=\int_{vol}[B]^T[D][B]d(\text{vol}),\{F_e^{th}\}=\int_{vol}[B]^T[D]\{\varepsilon^{th}\}d(vol)$$

$$[D]=\frac{E}{(1+v)(1-2v)}\begin{bmatrix}1-v & v & v & 0 & 0 & 0\\ v & 1-v & v & 0 & 0 & 0\\ v & v & 1-v & 0 & 0 & 0\\ 0 & 0 & 0 & \frac{1-2v}{2} & 0 & 0\\ 0 & 0 & 0 & 0 & \frac{1-2v}{2} & 0\\ 0 & 0 & 0 & 0 & 0 & \frac{1-2v}{2}\end{bmatrix}$$

- Parametrized form of a finite element model reads:

$$\Sigma_N:\begin{cases}\underbrace{(K_0+E\cdot K_1)}_{:=K(E)}\cdot U=\underbrace{(B_0+E\cdot B_1)}_{:=B(E)}\cdot u(t)\\ y=C\cdot U\end{cases}$$

- The transfer function reads: $G(E)=\frac{Y(s)}{U(s)}=C[K_0+E\cdot K_1]^{-1}\cdot(B_0+E\cdot B_1)$.
- Reduced system via Galerkin approximation reads:

$$\Sigma_r:\begin{cases}\underbrace{V^T(K_0+E\cdot K_1)V}_{:=K_r(E)}\cdot x(t)=\underbrace{V^TB}_{B_r}\cdot u\\ y=\underbrace{CV}_{C_r}\cdot x(t)\end{cases}$$

With projection subspace: $colspan\{V\}=\mathcal{K}_r\{-[K(E_0)]^{-1}\cdot K_1,[K(E_0)]^{-1}\cdot B\}$ we match the single-variable derivatives in Taylor Expansion of $G(E)$ and the corresponding $G_r(E)$[1]- [3].

- Multiple parameter system reads:

$$\Sigma_N:\begin{cases}\underbrace{(K_0+E_1\cdot K_1++E_2\cdot K_2+\cdots+E_p\cdot K_p)}_{K(E)}\cdot x=\\ \underbrace{(B_0+E_1\cdot B_1+E_2\cdot B_2+\cdots+E_p\cdot B_p)}_{B(E)}\cdot u(t)\\ y=C\cdot x\end{cases}$$

NUMERICAL RESULTS

We start with system level simulation, which considers Young's moduli of two different materials (silicon chip and solder material) as parameters. The setup is schematically displayed in Fig. 2.

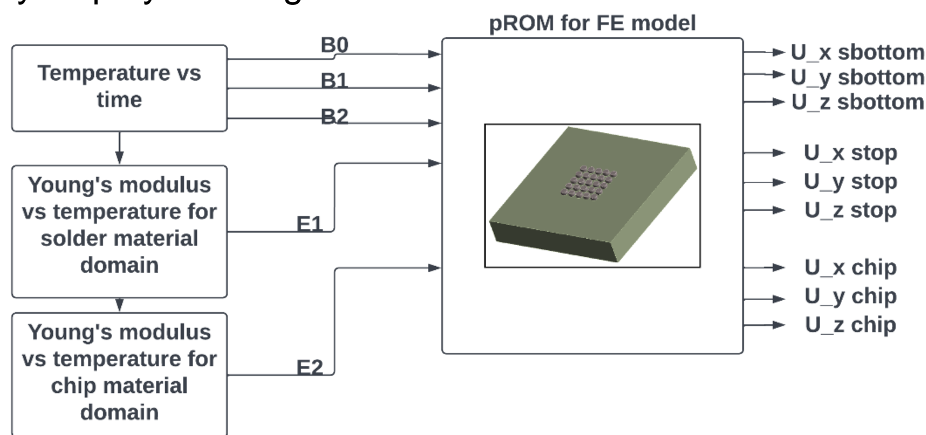

Fig. 2. A schematic for the system level simulation.

The time response to the temperature cycling with temperature dependent Young's moduli is shown in Fig. 3 and Tab. 1

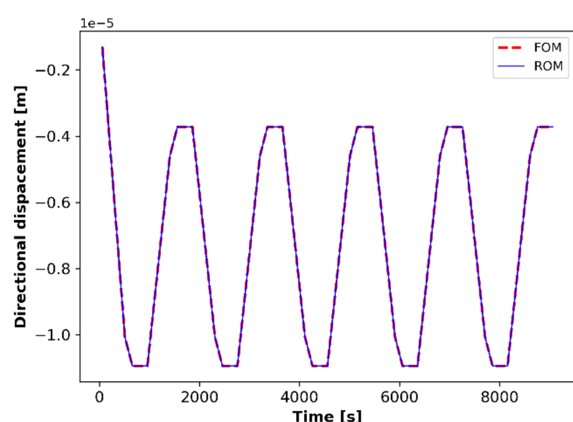

Fig. 3. A comparison between the full (FOM) and the reduced order model (ROM) with 252690 and 86 degrees of freedom (DOF), respectively.

Tab. 1. Time comparison between reduced and full order models at Intel Core Processor (Broadwell) @3.0 GHz, 64 GB.

Model	DOF	Time[s]
Finite element model	252690	2058.9
pROM generation (offline)	86	32.208
pROM (Online)	86	0.1600

Fig. 4 shows that the reduced model is a good approximation of the full one over a certain range of parameter in the vicinity of the chosen expansion point 2.9E10.

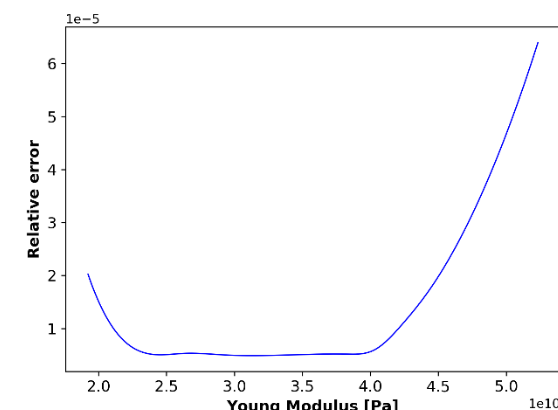

Fig. 4. Error plot for different Young's modulus verification values.

In Fig. 5 we studied the influence of the choice of the extraction point for the Young's modulus in the chip material domain. Also the influence of the size of reduced order model is investigated.

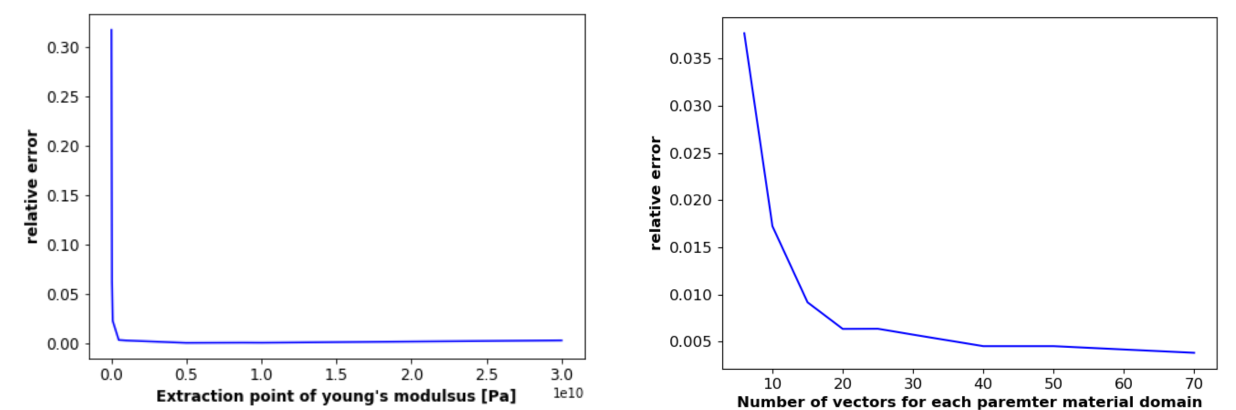

Fig. 5. A study of the influence of the extraction point choice and subspace size.

CONCLUSIONS AND OUTLOOK

- Young's modulus is preserved as a parameter in the reduced space. So in mechanical simulation that has a heat load and temperature depended parameter can be simulated and optimized in the reduced space.
- It's a middle step towards a full nonlinear reliability simulations to be reduced.

LITERATURE

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